FULL PAPER

High-Performance, Air-Stable, Top-Gate, p-Channel WSe_2 Field-Effect Transistor with Fluoropolymer Buffer Layer

*Seyed Hossein Hosseini Shokouh, Pyo Jin Jeon, Atiye Pezeshki, Kyunghee Choi, Hee Sung Lee, Jin Sung Kim, Eun Young Park, and Seongil Im**

High-performance, air-stable, p-channel WSe_2 top-gate field-effect transistors (FETs) using a bilayer gate dielectric composed of high- and low-*k* dielectrics are reported. Using only a high-k Al_2O_3 as the top-gate dielectric generally degrades the electrical properties of p-channel WSe_2, therefore, a thin fluoropolymer (Cytop) as a buffer layer to protect the 2D channel from high-*k* oxide forming is deposited. As a result, a top-gate-patterned 2D WSe_2 FET is realized. The top-gate p-channel WSe_2 FET demonstrates a high hole mobility of 100 $cm^2 V^{-1} s^{-1}$ and a I_{ON}/I_{OFF} ratio > 10^7 at low gate voltages (V_{GS} ca. −4 V) and a drain voltage (V_{DS}) of −1 V on a glass substrate. Furthermore, the top-gate FET shows a very good stability in ambient air with a relative humidity of 45% for 7 days after device fabrication. Our approach of creating a high-*k* oxide/low-*k* organic bilayer dielectric is advantageous over single-layer high-*k* dielectrics for top-gate p-channel WSe_2 FETs, which will lead the way toward future electronic nanodevices and their integration.

1. Introduction

As the scaling down of silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs) has almost reached its limit (<5 nm),[1] researchers have recently explored alternative atomically thin materials with large bandgaps and high mobility. In this context, semiconducting transition metal dichalcogenides (TMDs) have attracted much attention. TMDs not only have "graphene-like" properties, such as relatively high carrier mobility, mechanical flexibility, and chemical/thermal stability, but also exhibit "graphene-unlike" properties because of their discrete bandgap,[2,3] which may induce clear on/off switching behavior in devices. Because of their extreme scalability down to the monolayer and their van der Waals epitaxial structure without surface dangling bonds, TMD-based field-effect transistors (FETs) are immune for the short-channel effect and also show hardly any carrier-mobility degradation by surface oxidation-induced scattering.[4,5] MoS_2 is probably one of the most well-known TMDs because of the ease in finding natural molybdenite crystals.[2,6] Although there are a few reports about p-channel MoS_2 (FETs),[7–10] MoS_2 generally is n-doped, which makes it difficult to integrate both devices with p- and n-type conduction on the same flake.[11–15] On the other hand, WSe_2, another member of the TMD family has ambipolar conducting properties, which has resulted in a lot of attention recently.[16–20] This important property of WSe_2 promises the possibility for designing and fabricating integrated circuits on a single WSe_2 flake assuming both n-and p-type WSe_2 devices can be achieved by gate patterning with good performances and ambient stability.[21,22] So far, high electron and hole mobilities have been reported respectively from n- and p-type WSe_2 bottom-gate FETs, which were fabricated with proper metal contact and chemical doping methods.[1,23–29] Yet, the two practical issues with their ambient stability and gate patterning remain unresolved, although some groups have demonstrated air-stable, p-doping up to the degenerate limit.[26,27] In particular, studies on gate-patterned p-type WSe_2 FETs are still rare for both top- or bottom-gated devices, although gate-patterned FETs are a stepping-stone to realize integrated devices (see Table S1 in the Supporting Information for details).

In the present study, we have attempted a novel approach to achieve ambient, stable, high-performance, top-gate, patterned WSe_2 FETs both on SiO_2/p^+-Si and glass substrates. For this, we used a bilayer gate dielectric composed of high-*k* Al_2O_3 and a low-k organic fluoropolymer (Cytop) layer, which are respectively used for channel charging and as protection buffer. Using only a high-*k* Al_2O_3 as the top-gate dielectric has been known to degrade the electrical properties of p-channel WSe_2 FETS because of two major problems: The first relates to the fact that some of the hydrogen atoms (H) diffuse from the high-*k* Al_2O_3 into the WSe_2 channel during the atomic layer deposition (ALD) process, and the second is the occurrence of surface optical phonon scattering, which is enhanced by the high-*k* dielectric but the scattering can be attenuated by a low-k buffer.[30] Therefore, considering those two particular problems motivated us to investigate a thin low-*k* Cytop polymer as a proper buffer layer between the high-k Al_2O_3 and the WSe_2 channel. As a result, we realized a top-gate-patterned 2D WSe_2 FET on glass, which demonstrated a maximum hole mobility of 100 $cm^2 V^{-1} s^{-1}$ and

Dr. S. H. Hosseini Shokouh, P. J. Jeon, A. Pezeshki, K. Choi, Dr. H. S. Lee, J. S. Kim, E. Y. Park, Prof. S. Im
Institute of Physics and Applied Physics
Yonsei University
50 Yonsei-ro, Seodaemun-gu, Seoul 120-749, Korea
E-mail: semicon@yonsei.ac.kr

DOI: 10.1002/adfm.201502008

an I_{ON}/I_{OFF} ratio of >10^7 at a low gate voltage (V_{GS} ca. −4 V) and a drain voltage of V_{DS} = −1 V. Our device maintained its initial properties without significant changes under ambient air with a relative humidity of 45% for 7 days after device fabrication.

2. Results and Discussion

A 3D schematic of our top-gate FET is shown in **Figure 1**a, where the mechanically exfoliated WSe_2 flake and the Pt source/drain (S/D) electrodes are displayed. We used a 20 nm-thin Cytop low-k organic layer to cover the whole area of the WSe_2 flake, which works as a buffer; a 30 nm-thick Al_2O_3 was ultimately deposited on the Cytop/WSe_2 by atomic layer deposition (ALD) for passivation and to achieve the high-*k* gate dielectric. As Cytop is known to have internal dipoles formed by the C–F bonds typically for fluoropolymers, as shown in the inset of Figure 1a, such dipoles in Cytop will influence any thin p-channel WSe_2 beneath in an electrostatic way. Here, we selected two WSe_2 nanoflakes with different thicknesses (4- and 9-layer (L), measured by atomic force microscopy (AFM)) as shown in Figure 1b,c. The insets of Figure 1b and c show the optical images of 4L (3 nm) and 9L (6 nm) flakes, which were taken before Cytop passivation. **Figure 2**a shows the drain current–gate voltage (I_D–V_{GS}) transfer curves of a bottom-gate FET with a 4L-thin WSe_2 channel on 285 nm-thick SiO_2/p^+-Si. In the pristine FET after rapid thermal annealing (RTA), the on-current of the 4L WSe_2 FET was around 7 μA. The on-current increased to more than 15 μA if a Cytop layer was deposited on top of the same bottom-gate FET with thin WSe_2 channel, and a large threshold voltage (V_{th}) shift of (+) 11 V was also observed. This can be ascribed to the fact that our Cytop fluoropolymer intrinsically has electric dipole-containing C–F bonds that can cause hole accumulation near the Cytop/WSe_2 interface.[31] As a result, the on-current of the p-channel 4L-thin WSe_2 FET increased, as was also supported by the I_D–V_{DS} output curves in Figure 2b, and it eventually causes the field-effect linear mobility to increase (from 60 to 80 $cm^2\ V^{-1}\ s^{-1}$ as seen in Figure 2c). As a linear and symmetric output curve in V_{DS} = ±1 V usually indicates an ohmic contact between the source/drain and the channel,[1] the linear mobility (μ) could be extracted from the transfer curve using the well-known equation

$$\mu = \frac{g_m}{C_{ox} V_D \left(\frac{W}{L}\right)} \quad (1)$$

where g_m is the transconductance, C_{ox} is the dielectric capacitance (12.1 nF cm^{-2}), and W and L are the channel width and length, respectively. However, such dipole-induced effects become minimal as a thick layer of WSe_2 is used. According to the transfer and output curves of the 9L-thick WSe_2 FET in Figure 2d,e, the Cytop deposition induces only a little increase in I_D and the field-effect mobility remains the same (150 $cm^2\ V^{-1}\ s^{-1}$) for both the FET with and without the Cytop layer (Figure 2f). Compared to the 4L-thin WSe_2 FET, the 9L-thick WSe_2 FET initially showed a much higher on-current of around 30 μA because the thick WSe_2 already has enough hole carriers, whose total number does not increase much by

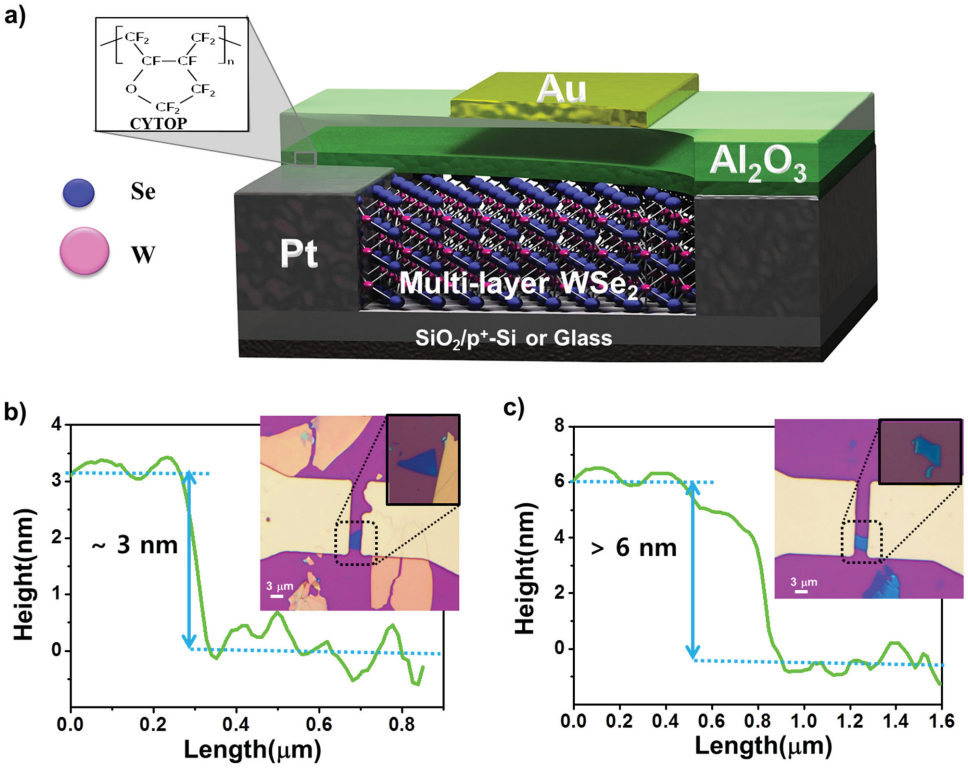

Figure 1. p-type WSe_2 top-gate FET: a) Schematic 3D view to show the inside of the top-gate FET with the bilayer Cytop/Al_2O_3 gate dielectric. b,c) AFM line profiles showing the thicknesses (3 and 6 nm, respectively) of the WSe_2 flakes as FET channels along with their optical images (insets).

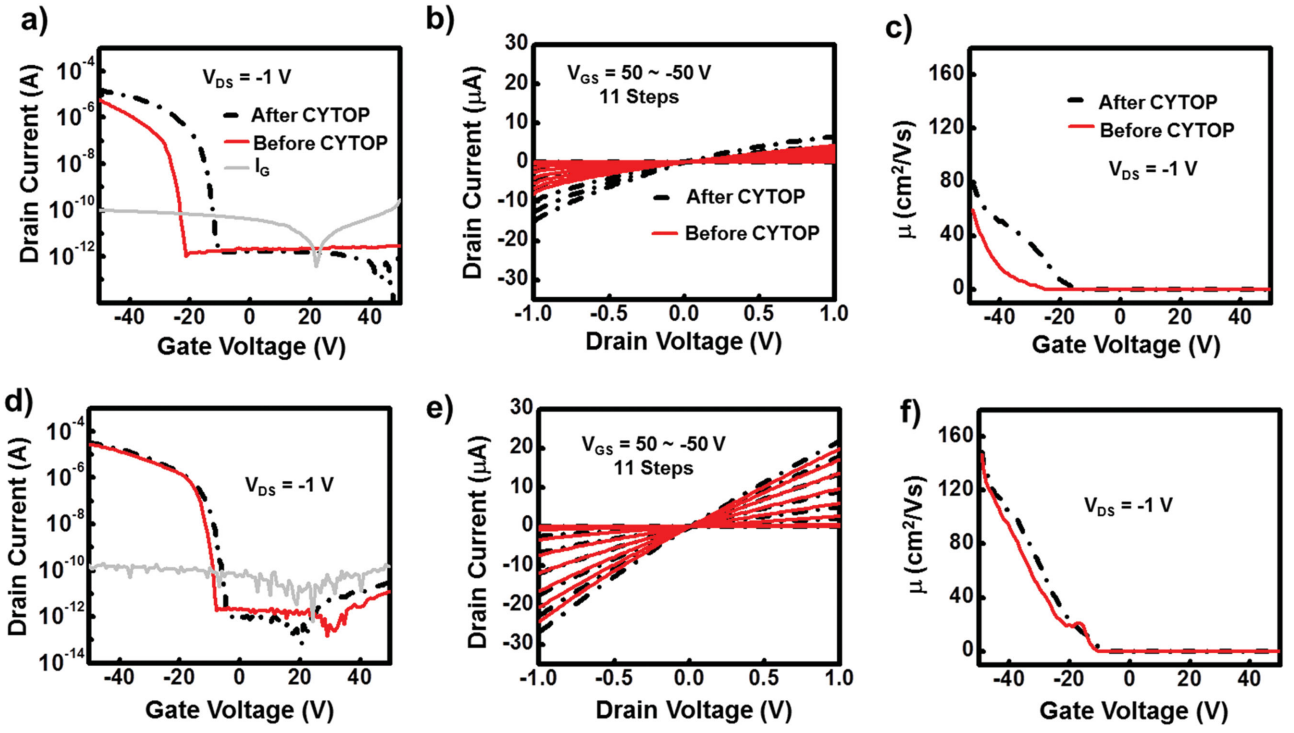

Figure 2. a–c) Transfer, output, and mobility curves of a bottom-gate FET based on a 4L WSe_2 flake. d–f) Transfer, output, and mobility curves of bottom-gate FET based on a 9L WSe_2. The red lines show the device properties before Cytop passivation whereas the black dashed line indicates the properties after Cytop passivation. The drain current in the transfer and output curves was normalized to the W/L ratio of the WSe_2 flakes for comparison purposes.

Cytop capping. By the way, this thickness-dependence behavior of the mobility is in agreement with a previous report on a bottom-gate FET with a 2D layered channel.[32–35] It should be noted that the drain current in the transfer and output curves in all figures are normalized to the W/L ratio of the WSe_2 flakes for better comparison.

In the next step, we deposited a 30 nm-thick Al_2O_3 layer as a high-k dielectric on top of the Cytop layer prior to the final top-gate electrode processing, and also examined the bottom-gate FET behavior using the oxide/Cytop bilayer. According to the transfer, output, and mobility behavior of the bottom-gate FETs with bilayer passivation as shown in **Figure 3**a–f, almost the same curves were obtained as those of Figure 2a–f for the FETs with only a single Cytop capping layer, regardless of the WSe_2 channel thickness. The mobility value slightly changed under the bilayer capping, but those changes were quite minimal. The more important finding was that Cytop functioned as a buffer layer to protect the WSe_2 channel from ALD processes and enable a high-k Al_2O_3, as clearly noted in Figure 3a; Al_2O_3 passivation alone could not stop the degradation of the electrical properties of the p-type WSe_2 FET. The output curves of our p-channel FET without a Cytop buffer showed only 40 nA as the I_D current in the inset of Figure 3b, thus giving rise to only a minimal mobility value, which was less than 1 $cm^2\ V^{-1}\ s^{-1}$ (inset of Figure 3c). We now suspect that the ALD-induced H atoms diffuse into the WSe_2 layer and react with the Se atoms to degrade the WSe_2 quality. However, in bottom-gate, n-channel WSe_2 FETs prepared with a Ti/Au contact instead of Pt, after passivation the diffusion of such H atoms during ALD processes improve the I_D current, as shown in Figure S1 in the Supporting Information. It thus seems that the diffused H may introduce additional charge traps,[2,36,37] such as Se vacancies, due to a chemical reaction of H_2Se,[38] whereas a thin layer of Cytop protects the channel from H diffusion to a degree. But more detailed studies are needed in the future to investigate this.

The bottom-gate FETs with 4L and 9L WSe_2 in Figure 3a–f were then converted into top-gate, p-channel FETs by patterning a Au gate electrode on top of the Al_2O_3/Cytop bilayer, as is shown in the inset of **Figure 4**c, and the electrical behavior of such top-gate FETs are displayed in Figure 4a–f. Due to the bilayer high dielectric-related capacitance (ca. 59 nF cm^{-2}, as calculated from the dual-gate structure;[39] see Figure S2, Supporting Information for details), a low gate voltage operation at around 4 V should be possible for these top-gate FETs as opposed to the high operation voltage of around 40 V needed for bottom-gate FETs (low dielectric capacitance of 12 nF cm^{-2}). The top-gate FET with a 4L WSe_2 channel showed a lower current of around 1 μA than the 2.5 μA obtained for the 9L WSe_2 FET, whereas both FETs displayed a similar V_{th} near 0 V and high on/off I_D ratios of over 10^6 ($I_{ON}/I_{OFF} > 10^6$ for 4L FET and $I_{ON}/I_{OFF} > 10^7$ for 9L FET at $V_{DS} = -1$ V). The maximum linear field-effect mobility of the FET with a 4L WSe_2 channel was around 6 $cm^2\ V^{-1}\ s^{-1}$, whereas that of FET with a 9L WSe_2 channel was around 25 $cm^2\ V^{-1}\ s^{-1}$. A slight mobility degradation at high-gate electric fields ($V_{GS} = -4$ V) was observed for the 4L FET whereas the 9L FET did not show such degradation. This is probably because the charge scattering near the

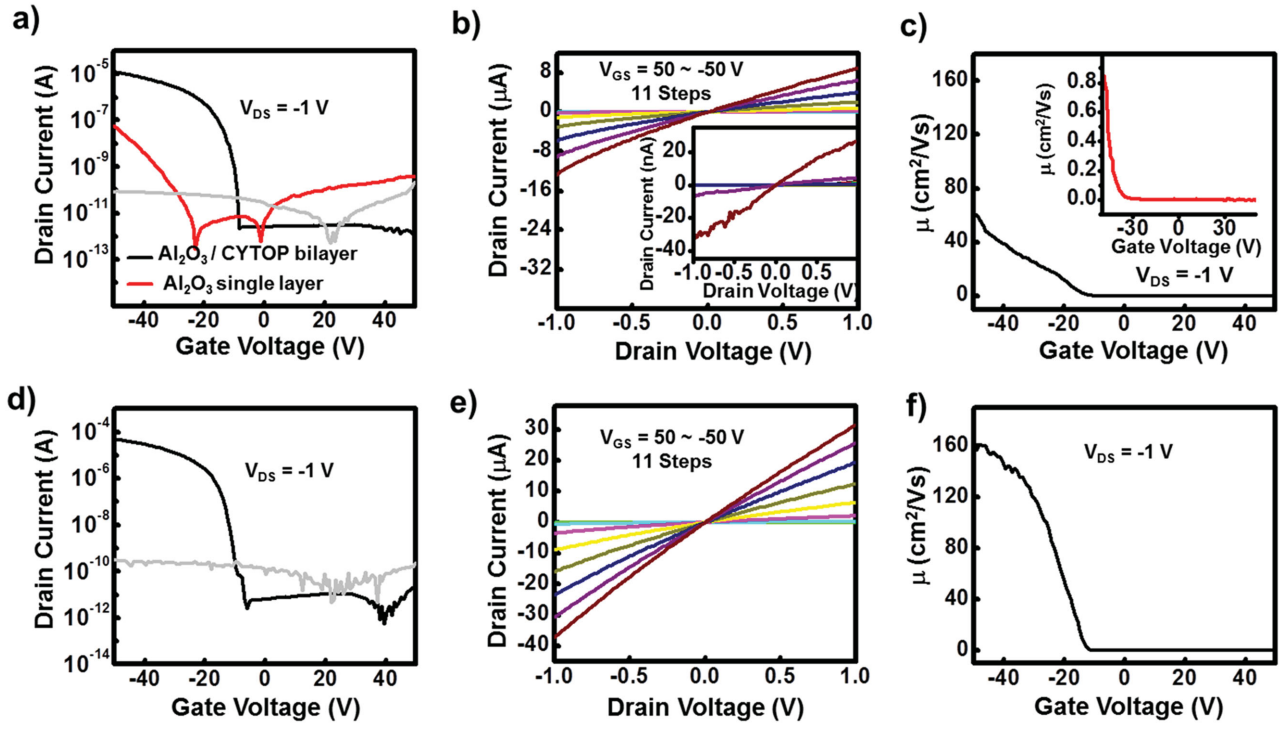

Figure 3. a) Transfer curve of a 4L WSe_2 bottom-gate FET after Al_2O_3 passivation with and without a Cytop buffer layer. b) Output curves of a 4L WSe_2 bottom-gate FET with Cytop buffer and Al_2O_3 passivation. Inset: output curves of a 4L WSe_2 bottom-gate FET with Al_2O_3 passivation only. c) Mobility of a 4L WSe_2 bottom-gate FET with Cytop buffer and Al_2O_3 passivation. Inset: mobility of the 4L WSe_2 bottom-gate FET without Cytop buffer layer but Al_2O_3 passivation only. d–f) Transfer, output, and mobility plots of a bottom-gate FET based on a 9L WSe_2 with Cytop buffer and Al_2O_3 passivation.

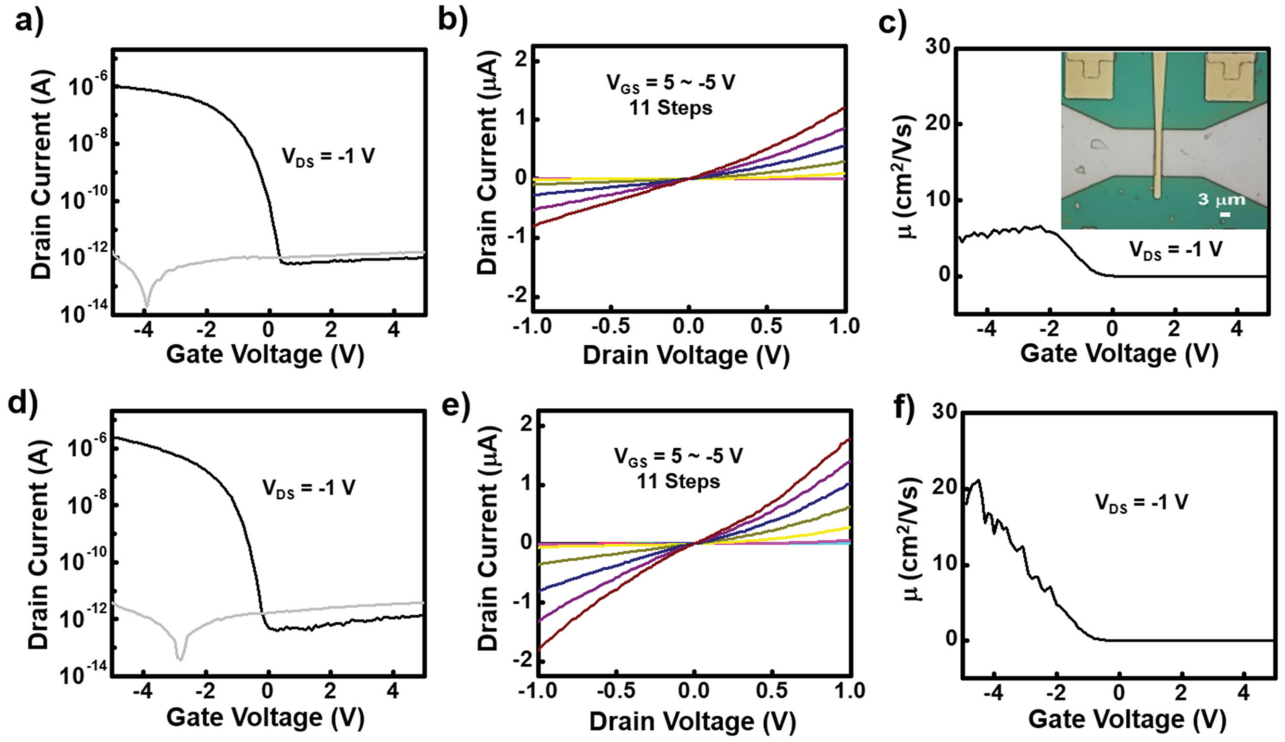

Figure 4. a–c) Transfer, output, and mobility curves of a top-gate FET with a 4L WSe_2 channel. The inset in (c) shows the optical image of our top-gate FET with the bilayer dielectric, which was fabricated on SiO_2/p^+-Si. d–f) Transfer, output, and mobility plots of the top-gate FET based on a 9L WSe_2.

channel/top dielectric interface was more of a problem in the thinner flake 2D channel than in the thicker one under high-gate fields; as a thicker channel is more conductive and induces less charge-scattering below the charge-accumulation layer near the interface under a high-gate induced electric field.[33]

As the mobility and the I_{ON}/I_{OFF} properties were higher in the FETs with thicker WSe_2 channels for both the bottom-gate and top-gate FETs, we then used the 9L WSe_2 FET to repeat the top-gate FET fabrication on a glass substrate (see the image in **Figure 5**d), and simultaneously to examine the ambient air stability of our top-gate FETs. According to Figure 5a–c, the transfer, output, and mobility behavior of the top-gate 9L WSe_2 FET on a glass substrate is quite similar to the behavior of the FET on a SiO_2/p^+-Si substrate (see Figure 4d–f), showing a mobility of around 23 $cm^2\ V^{-1}\ s^{-1}$. We measured the aging properties of this device for a duration of 10 days in ambient air with a relative humidity of 45%. For the first 7 days, the V_{th} of the FET barely changed, as seen in the transfer curves, although a slight increase in I_D was observed in the output curves along with a small increase in the mobility (up to ca. 30 $cm^2\ V^{-1}\ s^{-1}$). However, a clear 1 V shift of V_{th} toward the more positive side was seen after 10 days of aging in ambient air, which brought about an obvious increase in I_D of about three times and a mobility increase to 36 $cm^2\ V^{-1}\ s^{-1}$. The reason for the increase in the I_D current during aging, may be the W oxidation-induced p-doping by oxygen atoms,[40] which can diffuse through the layer in spite of our bilayer passivation; such hole-density increase due to oxygen diffusion has been reported before for p-type, organic, top-gate FETs with the same bilayer gate dielectric.[41–44] However, we believe that further studies such as Raman spectroscopy characterizations are required to verify this issue for 2D-layer TMDs based on WSe_2 and we may conclude that our Al_2O_3/Cytop bilayer was very helpful indeed but not absolutely perfect for passivating the WSe_2 surface.

As a final experiment to maximize the mobility of our 2D top-gate WSe_2 FETs on glass (see image in the inset of **Figure 6**c), we made FETs with even thicker WSe_2 flakes. According to the transfer, output, mobility, and AFM data in Figure 6a–d, the thickness of the 2D channel was around 8 nm (12 L), and the on-current and mobility of this FET were respectively 20 μA and 100 $cm^2\ V^{-1}\ s^{-1}$ at $V_{DS} = -1$ V. Such a high mobility has rarely been reported for top-gate WSe_2 FETs at low V_{GS}, and we recognize that the 12L-thick WSe_2 channel induced an I_D that was an order of magnitude higher than that of the 9L-thin WSe_2 FETs. This increase in I_D can be attributed to the thicker hole-conducting channel although such thick channels also cause more positive V_{th} (3 V) values and larger subthreshold swing values (400 mV dec^{-1}) as were seen in the 12L-thick WSe_2 FET as opposed to those of the 9L-thin WSe_2 device (–0.5 V, 200 mV dec^{-1}). According to recent results in the literature, 12L

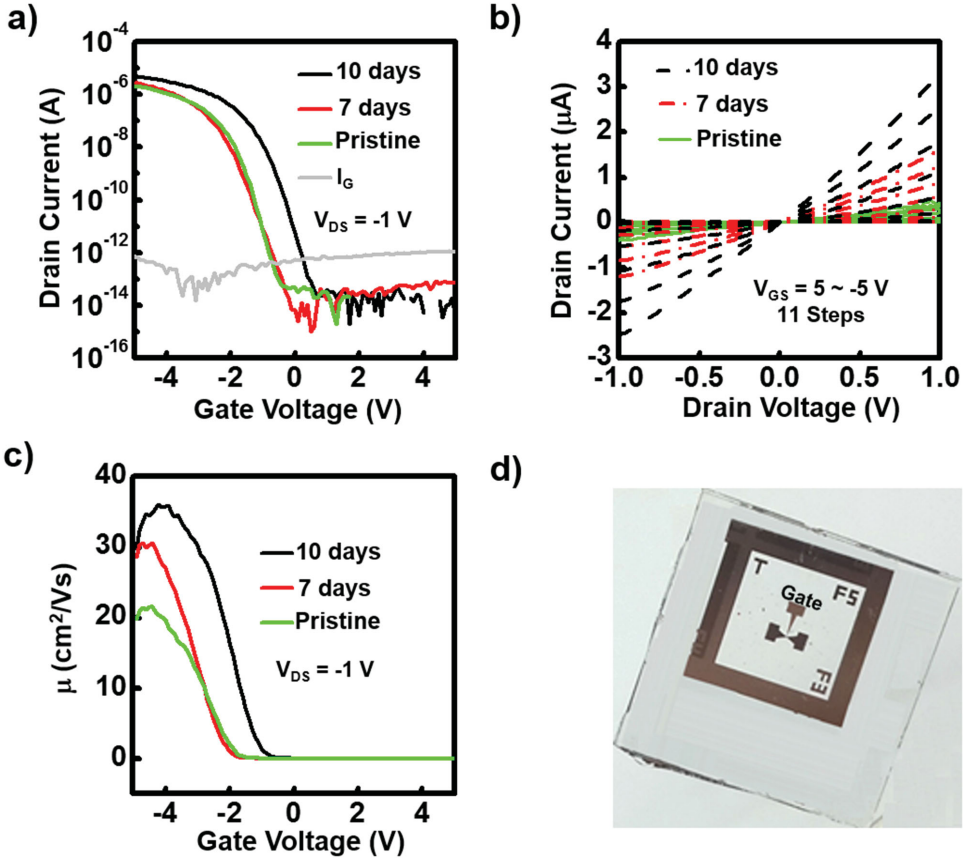

Figure 5. a–c) Transfer, output, and mobility behavior of the top-gate 9L WSe_2 FET on a glass substrate. The green lines indicate the electrical property of the pristine device whereas the black and red lines show the properties of the same device 7 and 10 days after fabrication, respectively. d) Photography image of the top-gate FET fabricated on a glass substrate.

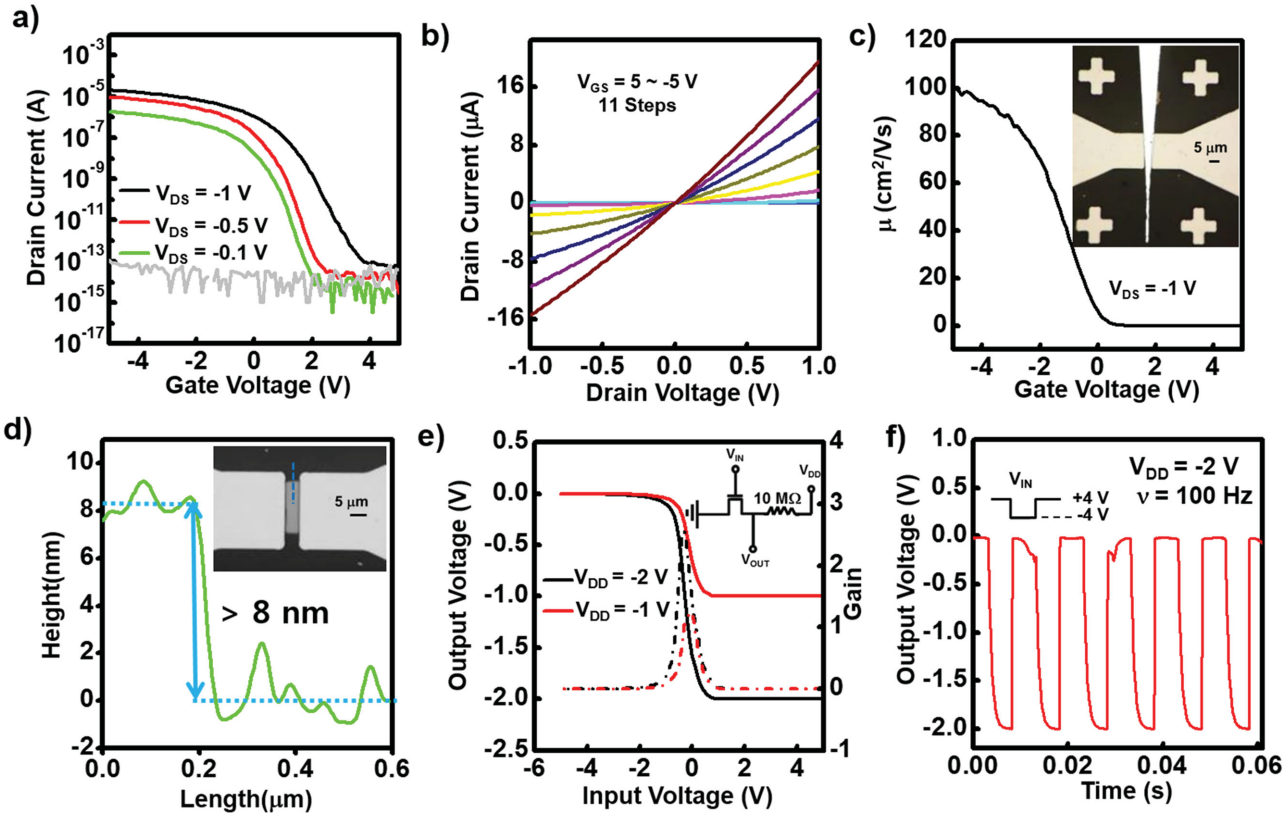

Figure 6. a) Transfer curve of a top-gate 12L WSe_2 FET on a glass substrate at V_{DS} of –0.1, –0.5, and –1 V. b) Output and c) mobility plots of a top-gate 12L WSe_2 FET on a glass substrate. The inset in (c) is an optical image. d) AFM line profile showing the thickness (8 nm) of the WSe_2 flake, shown in the inset. e) Voltage–transfer curves (VTC) of a logic inverter using a 10 MΩ external resistor (inset circuitry) with overlaid voltage gain plots (max. gain ca. 2.5) at V_{DD} of –1 and –2 V. f) Output voltage dynamics with square-wave input between +4 V (max) and –4 V (min) at 100 Hz, acquired at a V_{DD} of –2 V.

might be an optimal thickness for the WSe_2 channel in a bottom-gate FET,[35] which may work in top-gate WSe_2 FETs as well. To show more practical applications of this FET, we set up a logic inverter using a 10 MΩ external resistor, and measured the voltage-transfer curves (VTC), plotting the voltage gain (max. gain around 2.5), as shown in Figure 6e. A dynamic input voltage switching was observed with the inverter circuitry shown in the inset of Figure 6e. According to the time-domain plot in Figure 6f, the dynamic switching at 100 Hz showed the full –2 V output signal in 2 ms, measured at a supply voltage V_{DD} of –2 V with a square wave input voltage V_{IN} between +4 V (max) and –4 V (min).

3. Conclusion

We have fabricated a p-type, WSe_2 top-gate FET using a bilayer gate dielectric composed of a high- and low-*k* dielectric both on SiO_2/p^+-Si and glass substrates. Using only a high-*k* Al_2O_3 layer as the top-gate dielectric generally degrades the electrical property of p-channel WSe_2 FETs. Therefore, we deposited a thin fluoropolymer as a buffer layer to protect the 2D channel from the high-*k* oxide forming process. As a result, we successfully realized a top-gate-patterned 2D WSe_2 FET. Our top-gate, p-channel WSe_2 FET demonstrated a high hole mobility of 100 cm^2 V^{-1} s^{-1} and an I_{ON}/I_{OFF} ratio of $>10^7$ at a low gate voltage V_{GS} of –4 V and a drain voltage V_{DS} of –1 V on a glass substrate. Furthermore, the top-gate FET showed a very good stability in ambient air with a relative humidity of 45% for 7 days after device fabrication. We conclude that our approach of using a high-*k* oxide/low-*k* organic bilayer dielectric for top-gate, p-channel, WSe_2 FETs may show the way for future electronic nanodevices and their integration.

4. Experimental Section

Device Fabrication: To fabricate the p-type WSe_2 top-gate FET, we used a bilayer gate dielectric composed of a high- and low-*k* dielectric. A p^+-Si/SiO_2 wafer was ultrasonically cleaned in acetone, methyl alcohol, and de-ionized water, to be used as a substrate. Bulk WSe_2 crystals were exfoliated by adhesive tape (known as micromechanical exfoliation) on either a 285 nm-thick SiO_2/p^+-Si or glass substrate. Tape residue was removed by soaking in acetone, followed by a methyl alcohol rinse, and drying under a N_2 flow. Then we searched for appropriate few-layer WSe_2 flakes using an optical microscope. In fact, each flake shows a distinctive optical contrast depending on the layer thickness, as shown in the optical microscopy (OM) images that are inserted in Figure 1b,c. The S/D electrodes were patterned using a conventional photolithography process. Then, to form the universal back-gate FETs a 25 nm-thin Pt and a 25 nm-thin Ti layer (Ti/Pt) were deposited on the WSe_2 (Pt–WSe_2 contacts) as the ohmic source–drain (S/D) contacts using DC magnetron sputtering. For the lift-off process, acetone and lift of layer (LOL) remover were used, followed by rapid thermal annealing (RTA) at 250 °C for 10 minutes to make the ohmic connection for p-type FETs. After source/drain fabrication, a 20-nm thick conventional fluoropolymer Cytop (Asahi

glass, CTX-809M) was spin-coated (followed by curing at 100 °C for 30 min in an oven). A 30 nm-thick Al_2O_3 layer was deposited as a high-k gate dielectric after Cytop passivation by atomic layer deposition (ALD) at 100 ° C. Finally, the gate electrode was patterned and realized using a photolithography process followed by deposition of a 50-nm Au layer by thermal evaporation. The same processes were carried out to fabricate p-type WSe_2 top-gate FETs on the glass substrate.

Electrical Measurements: All device characterizations were performed in the dark at room temperature using a semiconductor parameter analyzer (HP4155C, Agilent Technologies), and a function generator (AFG 310, Tektronix) was used for dynamic measurements on the WSe_2 flake FETs.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors acknowledge the financial support from the National Research Foundation of Korea (NRL program: grant no. 2014R1A2A1A01004815, Nano-Material Technology Development program: grant no. 2012M3A7B4034985) and the Brain Korea 21 plus Program. S.H.H.S. and P.J.J. contributed equally to this work.

Received: May 15, 2015
Revised: September 8, 2015
Published online: October 23, 2015

[1] W. Liu, J. Kang, D. Sarkar, Y. Khatami, D. Jena, K. Banerjee, *Nano Lett.* **2013**, *13*, 1983.
[2] H.-J. Chuang, X. Tan, N. J. Ghimire, M. M. Perera, B. Chamlagain, M. M.-C. Cheng, J. Yan, D. Mandrus, D. Tománek, Z. Zhou, *Nano Lett.* **2014**, *14*, 3594.
[3] H. Sahin, S. Tongay, S. Horzum, W. Fan, J. Zhou, J. Li, J. Wu, F. M. Peeters, *Phys. Rev. B: Condens. Matter* **2013**, *87*, 165.
[4] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, L. Colombo, *Nat. Nanotechnol.* **2014**, *9*, 768.
[5] H.-Y. Park, M.-H. Lim, J. Jeon, G. Yoo, D.-H. Kang, S. K. Jang, M. H. Jeon, Y. Lee, J. H. Cho, G. Y. Yeom, W.-S. Jung, J. Lee, S. Park, S. Lee, J.-H. Park, *ACS Nano* **2015**, *9*, 2368.
[6] D. Sarkar, W. Liu, X. Xie, A. C. Anselmo, S. Mitragotri, K. Banerjee, *ACS Nano* **2014**, *8*, 3992.
[7] S. Chuang, C. Battaglia, A. Azcatl, S. McDonnell, J. S. Kang, X. Yin, M. Tosun, R. Kapadia, H. Fang, R. M. Wallace, A. Javey, *Nano Lett.* **2014**, *14*, 1337.
[8] K. Dolui, I. Rungger, S. Sanvito, *Phys. Rev. B: Condens. Matter* **2013**, *87*, 165.
[9] M. R. Laskar, D. N. Nath, L. Ma, E. W. Lee, C. H. Lee, T. Kent, Z. Yang, R. Mishra, M. A. Roldan, J.-C. Idrobo, S. T. Pantelides, S. J. Pennycook, R. C. Myers, Y. Wu, S. Rajan, *Appl. Phys. Lett.* **2014**, *104*, 092.
[10] J. Suh, T.-E. Park, D.-Y. Lin, D. Fu, J. Park, H. J. Jung, Y. Chen, C. Ko, C. Jang, Y. Sun, R. Sinclair, J. Chang, S. Tongay, J. Wu, *Nano Lett.* **2014**, *14*, 6976.
[11] J. Y. Kwak, J. Hwang, B. Calderon, H. Alsalman, N. Munoz, B. Schutter, M. G. Spencer, *Nano Lett.* **2014**, *14*, 4511.
[12] H. S. Lee, S.-W. Min, Y.-G. Chang, M. K. Park, T. Nam, H. Kim, J. H. Kim, S. Ryu, S. Im, *Nano Lett.* **2012**, *12*, 3695.
[13] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nat. Nanotechnol.* **2011**, *6*, 147.
[14] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, M. S. Strano, *Nat. Nanotechnol.* **2012**, *7*, 699.
[15] F. M. Espinosa, Y. K. Ryu, K. Marinov, D. Dumcenco, A. Kis, R. Garcia, *Appl. Phys. Lett.* **2015**, *106*, 103.
[16] B. W. H. Baugher, H. O. H. Churchill, Y. Yang, P. Jarillo-Herrero, *Nat. Nanotechnol.* **2014**, *9*, 262.
[17] R. Bratschitsch, *Nat. Nanotechnol.* **2014**, *9*, 247.
[18] S. Das, J. Appenzeller, *Appl. Phys. Lett.* **2013**, *103*, 103.
[19] A. Pospischil, M. M. Furchi, T. Mueller, *Nat. Nanotechnol.* **2014**, *9*, 257.
[20] J. S. Ross, P. Klement, A. M. Jones, N. J. Ghimire, J. Yan, D. G. Mandrus, T. Taniguchi, K. Watanabe, K. Kitamura, W. Yao, D. H. Cobden, X. Xu, *Nat. Nanotechnol.* **2014**, *9*, 268.
[21] S. Das, M. Dubey, A. Roelofs, *Appl. Phys. Lett.* **2014**, *105*, 083.
[22] M. Tosun, S. Chuang, H. Fang, A. B. Sachid, M. Hettick, Y. Lin, Y. Zeng, A. Javey, *ACS Nano* **2014**, *8*, 4948.
[23] K. Chen, D. Kiriya, M. Hettick, M. Tosun, T.-J. Ha, S. R. Madhvapathy, S. Desai, A. Sachid, A. Javey, *APL Mater.* **2014**, *2*, 092.
[24] H. Fang, M. Tosun, G. Seol, T. C. Chang, K. Takei, J. Guo, A. Javey, *Nano Lett.* **2013**, *13*, 1991.
[25] C.-H. Chen, C.-L. Wu, J. Pu, M.-H. Chiu, P. Kumar, T. Takenobu, L.-J. Li, *2D Mater.* **2014**, *1*, 034.
[26] D.-H. Kang, J. Shim, S. K. Jang, J. Jeon, M. H. Jeon, G. Y. Yeom, W.-S. Jung, Y. H. Jang, S. Lee, J.-H. Park, *ACS Nano* **2015**, *9*, 1099.
[27] P. Zhao, D. Kiriya, A. Azcatl, C. Zhang, M. Tosun, Y.-S. Liu, M. Hettick, J. S. Kang, S. McDonnell, S. Kc, J. Guo, K. Cho, R. M. Wallace, A. Javey, *ACS Nano* **2014**, *8*, 10808.
[28] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, A. Javey, *Nano Lett.* **2012**, *12*, 3788.
[29] H. Zhou, C. Wang, J. C. Shaw, R. Cheng, Y. Chen, X. Huang, Y. Liu, N. O. Weiss, Z. Lin, Y. Huang, X. Duan, *Nano Lett.* **2015**, *15*, 709.
[30] N. Ma, D. Jena, *Phys. Rev. X* **2014**, *4*, 011.
[31] P. J. Jeon, S.-W. Min, J. S. Kim, S. R. A. Raza, K. Choi, H. S. Lee, Y. T. Lee, D. K. Hwang, H. J. Choi, S. Im, *J. Mater. Chem. C* **2015**, *3*, 2751.
[32] S. Das, J. Appenzeller, *Phys. Status Solidi RRL* **2013**, *7*, 268.
[33] S. Das, J. Appenzeller, *Nano Lett.* **2013**, *13*, 3396.
[34] S. Das, H.-Y. Chen, A. V. Penumatcha, J. Appenzeller, *Nano Lett.* **2013**, *13*, 100.
[35] N. R. Pradhan, D. Rhodes, S. Memaran, J. M. Poumirol, D. Smirnov, S. Talapatra, S. Feng, N. Perea-Lopez, A. L. Elias, M. Terrones, P. M. Ajayan, L. Balicas, *Sci. Rep.* **2015**, *5*, 8979.
[36] S. M. George, A. W. Ott, J. W. Klaus, *J. Phys. Chem.* **1996**, *100*, 13121.
[37] B. Ryu, Y. T. Lee, K. H. Lee, R. Ha, J. H. Park, H.-J. Choi, S. Im, *Nano Lett.* **2011**, *11*, 4246.
[38] C. Tsai, K. Chan, F. Abild-Pedersen, J. K. Norskov, *Phys. Chem. Chem. Phys.* **2014**, *16*, 13156.
[39] M. S. Fuhrer, J. Hone, *Nat. Nanotechnol.* **2013**, *8*, 146.
[40] H. Liu, N. Han, J. Zhao, *RSC Adv.* **2015**, *5*, 17572.
[41] D. K. Hwang, C. Fuentes-Hernandez, M. Fenoll, M. Yun, J. Park, J. W. Shim, K. A. Knauer, A. Dindar, H. Kim, Y. Kim, J. Kim, H. Cheun, M. M. Payne, S. Graham, S. Im, J. E. Anthony, B. Kippelen, *ACS Appl. Mater. Interfaces* **2014**, *6*, 3378.
[42] D. K. Hwang, C. Fuentes-Hernandez, J. Kim, W. J. Potscavage, S.-J. Kim, B. Kippelen, *Adv. Mater.* **2011**, *23*, 1293.
[43] C.-Y. Wang, C. Fuentes-Hernandez, J.-C. Liu, A. Dindar, S. Choi, J. P. Youngblood, R. J. Moon, B. Kippelen, *ACS Appl. Mater. Interfaces* **2015**, *7*, 4804.
[44] M. Yamamoto, S. Dutta, S. Aikawa, S. Nakaharai, K. Wakabayashi, M. S. Fuhrer, K. Ueno, K. Tsukagoshi, *Nano Lett.* **2015**, *15*, 2067.